Discussion of QA Plan for DUNE/ SBND Cold Electronics

AUGUST 20TH, 2015

Outline

- Cold Electronics for SBND/DUNE
- Key Developments with Commonalities
- System Integration
  - MicroBooNE experience
  - SBND development
- FE/ADC Chip Production Plan
- Summary

Cold Electronics for SBND/DUNE

- SBND
  - ***11,264 channels (sense wires)***
  - 704 FE ASICs
  - 704 ADC ASICs
  - 88 cold FPGAs
  - 88 cold mother boards
  - 4 sets of cold cable
  - 4 sets of signal feed-through
  - 32 warm interface boards
- protoDUNE@CERN
  - ***15,360 channels***
  - 960 FE ASICs/960 ADC ASICs/ 120 cold FPGAs
  - 120 cold mother boards
  - 3 sets of cold cable
  - 3 sets of signal feed-through
- DUNE 10 kt
  - ***384,000 channels***
  - 24,000 FE ASICs/24,000 ADC ASICs/6,000 COLDATA ASICs
  - 3,000 cold mother boards
  - 75 sets of cold cable
  - 75 sets of signal feed-through

Key Developments with Commonalities

- Key Developments
  - TPC electrode system (resistive cathode, field cage, sense wire planes)
  - Cold electronics
    - FE ASIC
    - ADC ASIC
    - Cold FPGA and/or COLDATA ASIC
    - Cold mother board, connections to sense wires
  - Cold cables
  - Signal feed-through
- ***A program should be established to build a full cold readout system, from TPC electrode to the signal feed-through, for system tests of APA (at each step, following fabrication, transport and installation in the cryostat).***

System Integration

- Each key component will have a dedicated test stand and QA plan
  - This includes ASICs, boards, cables, feed-throughs, etc.
  - This has been done before for both ATLAS (~10,000 boards, ~150 feed-throughs & cables) and MicroBooNE (~2,000 ASICs, ~500 boards, ~13 feed-throughs & cables)
- ***Emphasis should be put on the system integration***
  - System integration is crucial to understand detector performance and finalize the design
  - Various integration tests have been done for both ATLAS (at BNL & CERN) and MicroBooNE (at BNL & Fermilab)
  - System integration, in both SBND and protoDUNE at CERN, will serve as crucial steps towards a successful construction of DUNE 10kton

Scale of Small LAr TPC Projects in SBN & DUNE

- MicroBooNE
  - ***8,256 channels***
  - 516 FE ASICs
  - 50 cold mother boards
  - 11 sets of cold cable (269)
  - 11 sets of signal feed-through
  - 269 warm interface boards
  - 11 sets of warm cable (258)
  - 129 receiver & ADC boards
- 35 ton
  - ***2,048 channels***
  - 128 FE ASICs
  - 128 ADC ASICs
  - 16 cold FPGAs
  - 16 cold mother boards

Importance of System Integration

- 35T test has shown the efforts of cold electronics development were seriously ***under***-estimated – especially the required manpower
  - On the contrary, the MicroBooNE cold electronics development has a larger scale but was delivered on time
- ***Integration test should be planned at an early stage***
  - To bring all components together at Fermilab at the last moment and hope it will work together, is only a good wish …
  - In-kind contributions from various institutes are very important, but not the way to solve the problem
  - Integration test stand should be developed and made available to other parts of the system , e.g. warm electronics, DAQ subsystem, etc.
- ***Put serious efforts on cabling and FT development***
  - Important components for system design and integration
  - Early prototype and system tests are necessary to avoid unexpected delay at later stage

QA of Cold Electronics Development

- ASIC Test Stand
  - Individual test stand for each ASIC
    - All ASICs should be screening tested individually at RT
  - ASIC cold test board to verify the yield of ASIC operating in cold
    - This will help determine if all ASICs need to go through the cold test
- Cold Electronics Board Test Stand
  - Focus on board level evaluation test
  - Simple readout and DAQ system for easy debug test
  - Can be re-purposed to the dedicated debug test station once the system integration test stand becomes available

QA of Cold Electronics Development

- System Integration Test Stand
  - Focus on system integration of various components
  - Complete system with golden setup can be used to test individual components, for both prototype production
    - Cold electronics board, cable, feed-through, warm interface board etc.
  - Multiple system integration test stands to serve different purposes

QA of Cold Electronics Development

- System Integration Test Stand
  - SBND
    - Test stand at BNL will focus on the FE evaluation test
    - Test stand at Nevis will focus on the BE evaluation test
    - Test stand at FNAL will focus on the DAQ development and detector integration
  - protoDUNE & DUNE 10kt
    - Test stand at BNL will focus on the FE evaluation test
    - ***protoDUNE*** – Test stand at CERN will focus on the BE evaluation test, DAQ development and detector integration
    - ***DUNE 10kt*** – Test stand at FNAL will focus on the DAQ development and detector integration

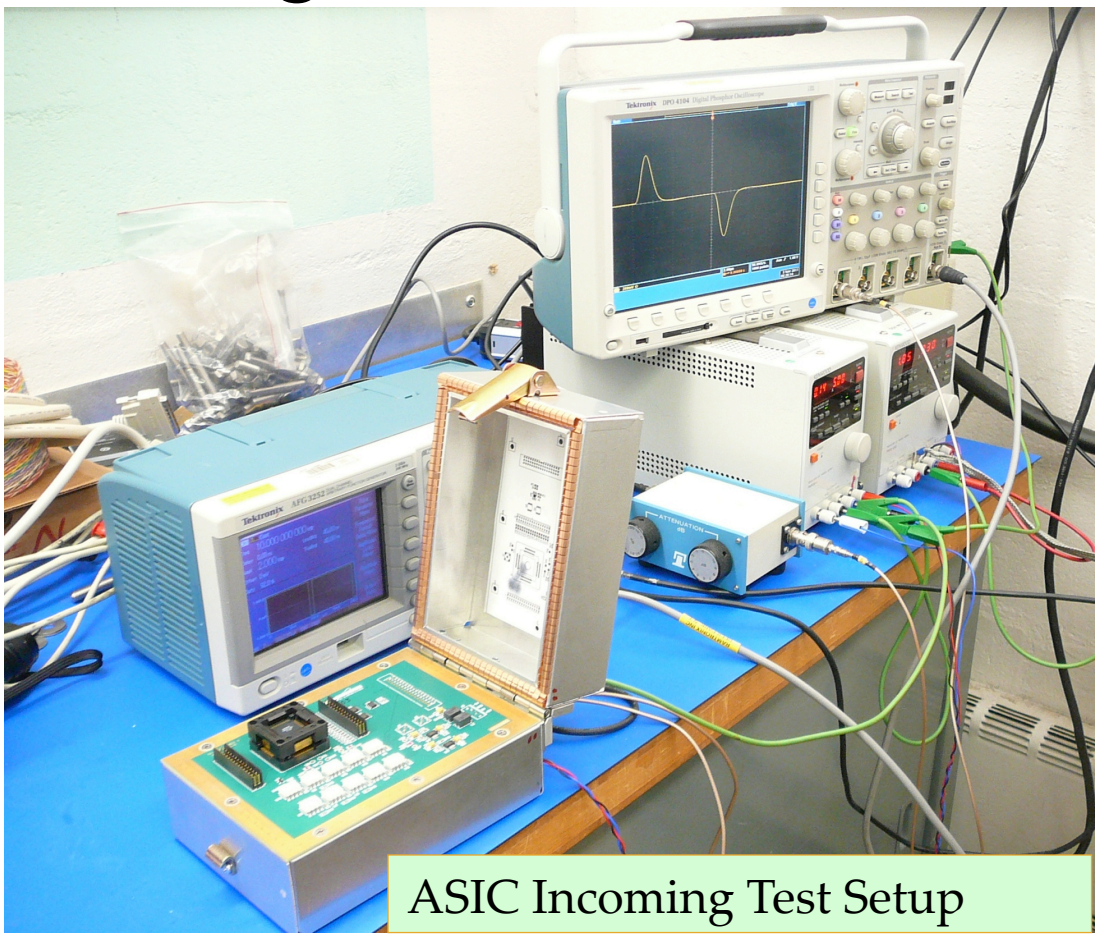
QA of Cold Electronics Development

- Integration test stands for SBND and protoDUNE are ***different***
  - Cold electronics boards, cold cable, signal feed-through, warm interface electronics, DAQ hardware are different for SBND and protoDUNE
  - Development of integration test stands can share the experience and expertise of developers
  - Separate test stands for SBND and protoDUNE should be built and maintained
- ASIC test stands can be shared between SBND and protoDUNE
- It is possible to share the simple readout and DAQ system for cold electronics board test stand between SBND and protoDUNE

MicroBooNE Experience

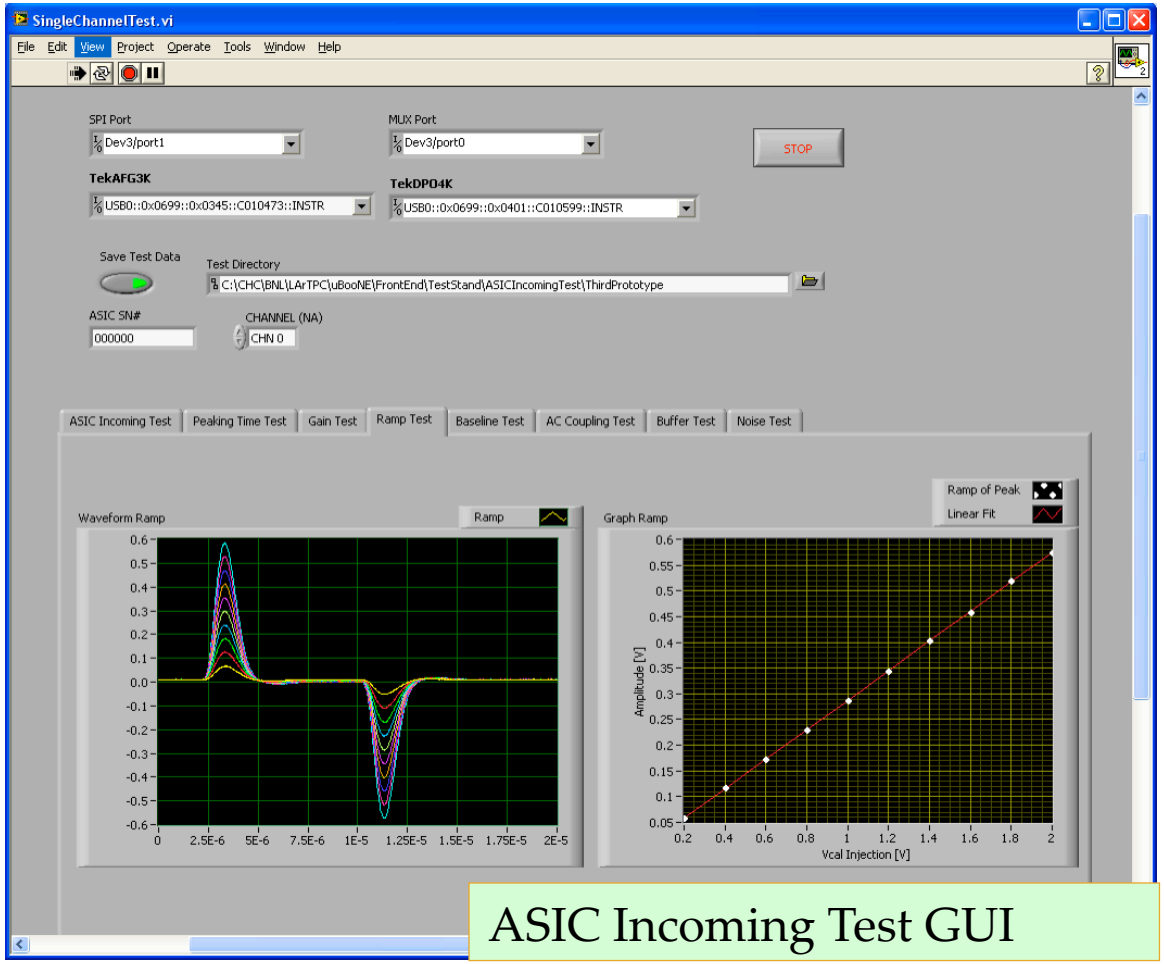
- The following slides show what has been done for MicroBooNE

ASIC Incoming Test Stand



ASIC Incoming Test Setup

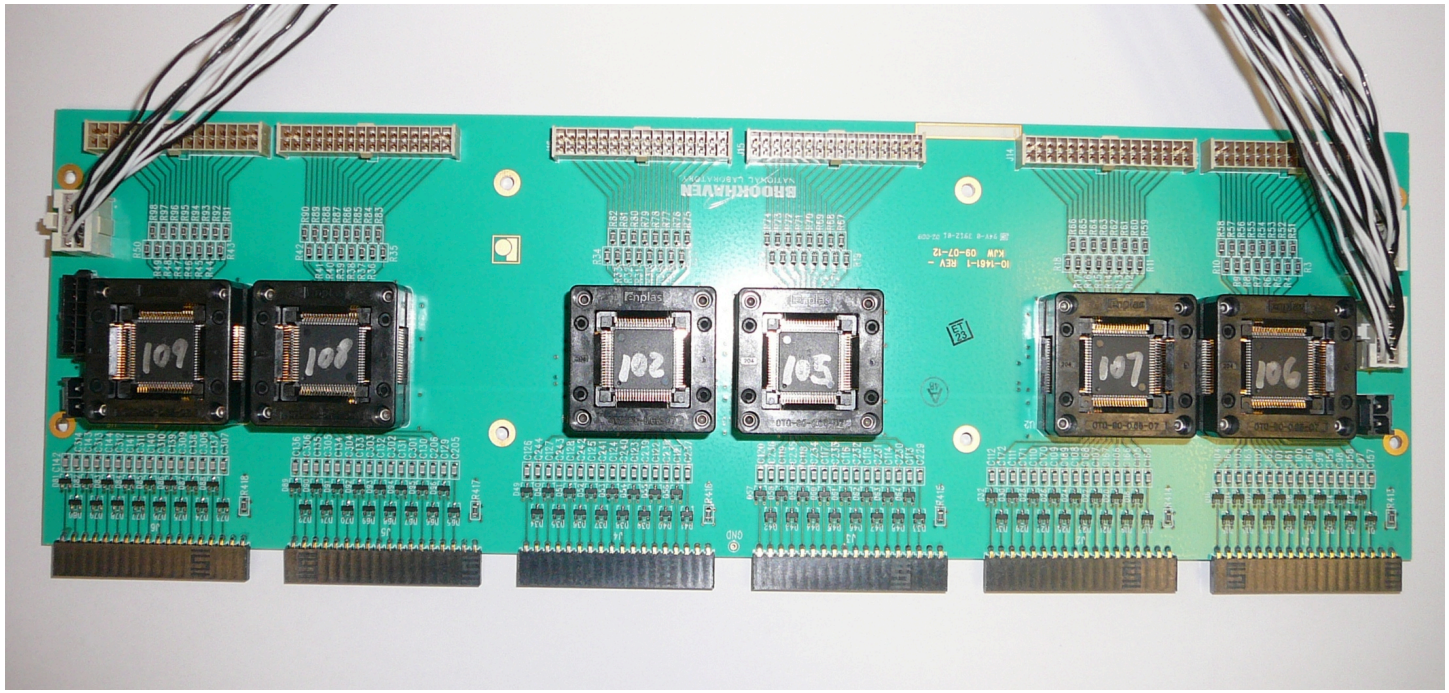
ASIC Incoming Test Stand



ASIC Incoming Test GUI

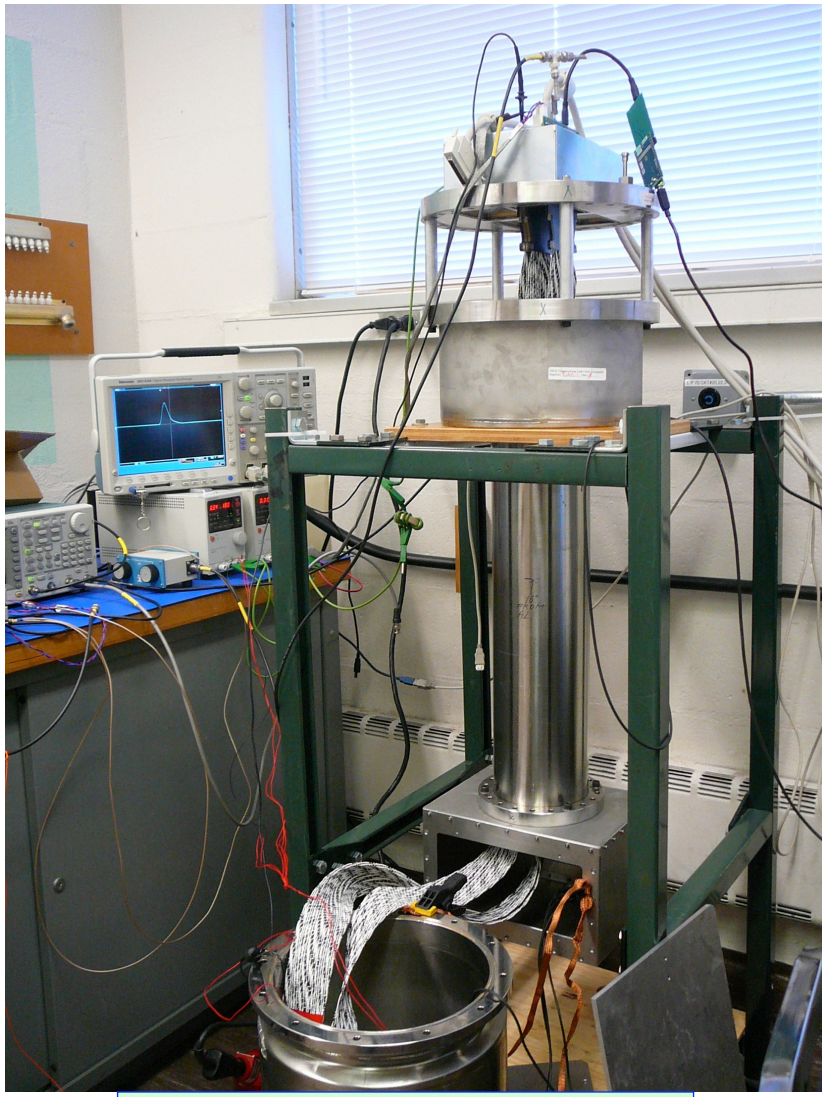
- All FE ASICs are fully qualified before populated on the cold mother boards

ASIC Cryo Test Board

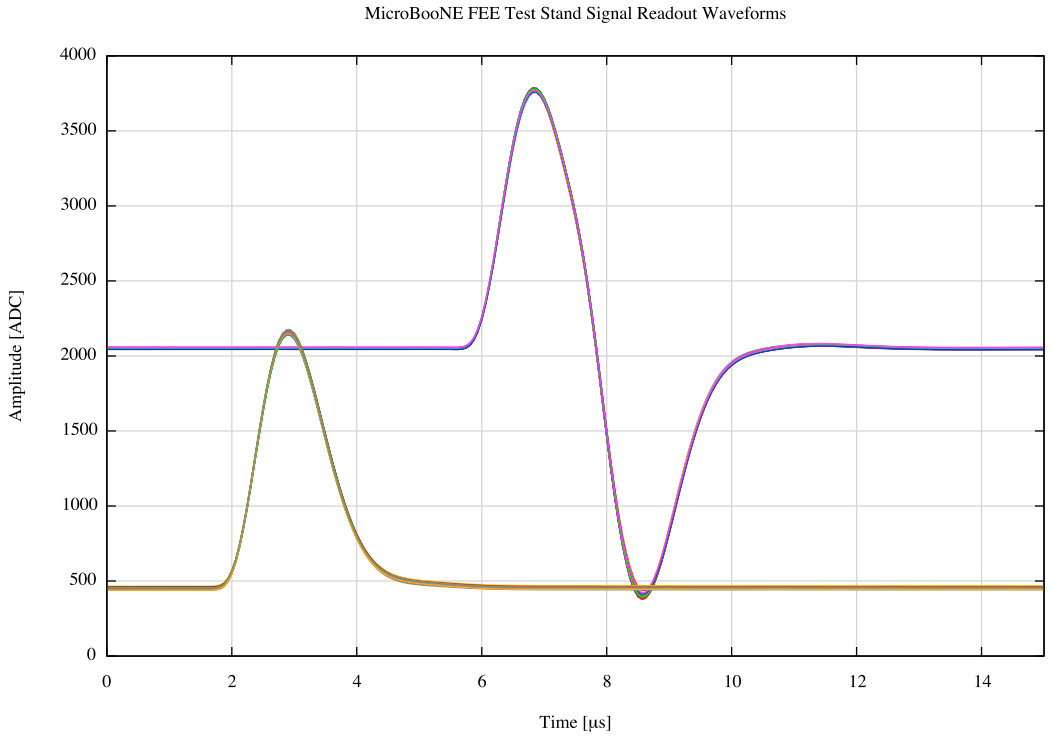


- Based on the test results of 201 ASICs in LN_2, it was decided not to continue the cold screening test on the rest of the chips; they will be tested cold, installed on the boards

MicroBooNE FEE Test Stand



Cold Test of FEE Test Stand



64 channels of signal chain response overlapped

Prototype 1 Integration Test Stand

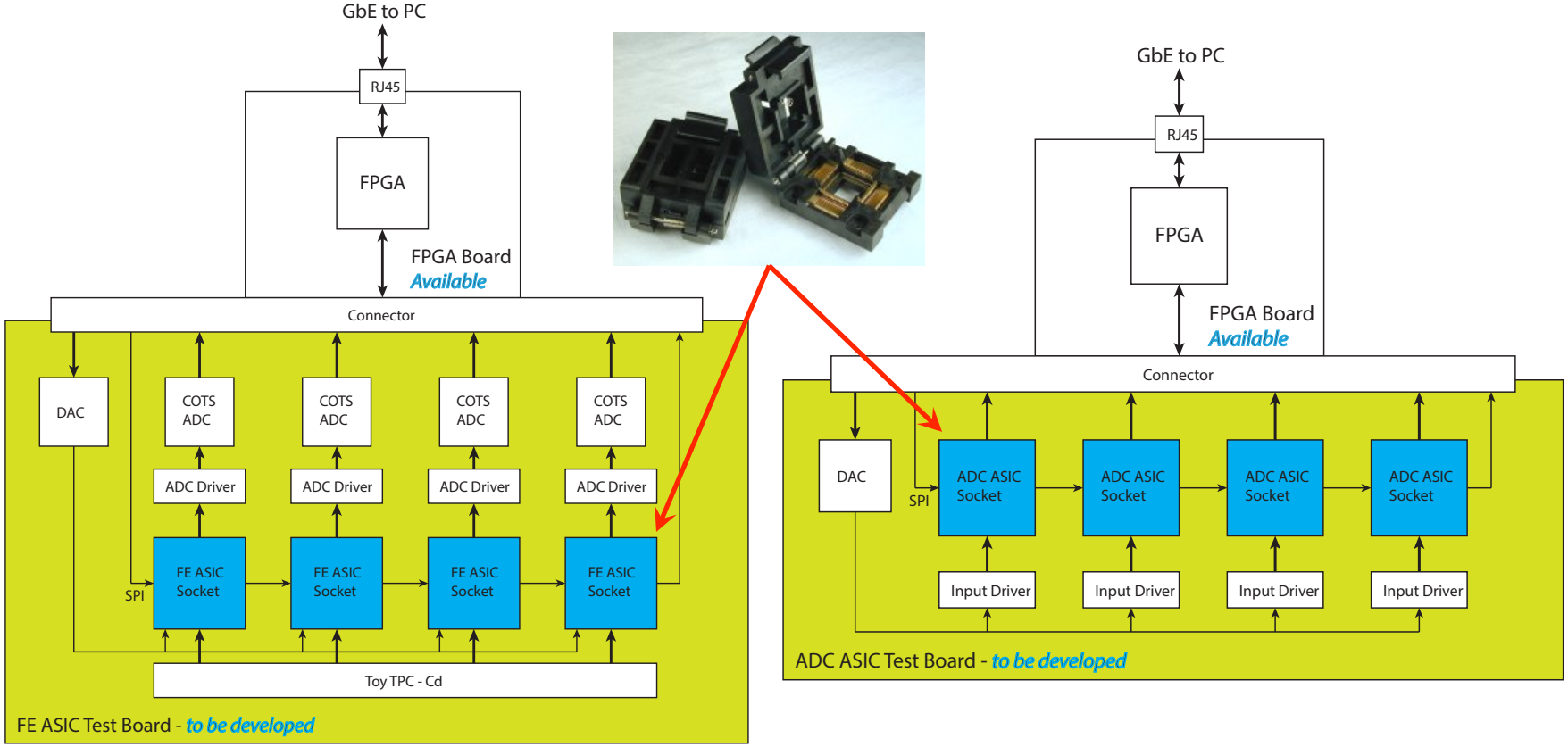
Prototype 2 Integration Test Stand

- Test stand at Nevis was later moved to FNAL for DAQ system development

SBND Development

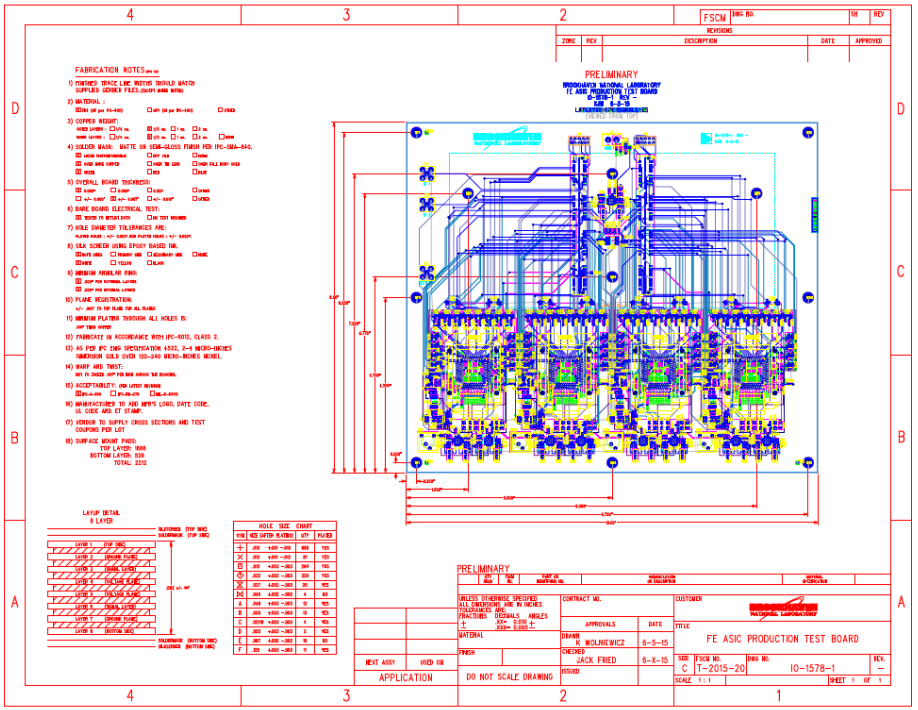
- The following slides show what is being done for SBND ASIC test

Cold Electronics



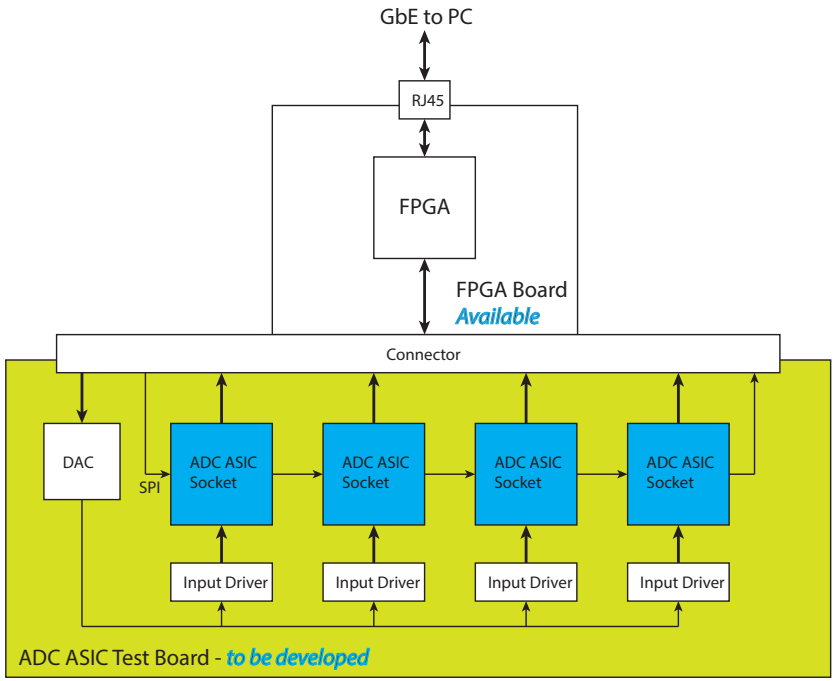
- ASIC Evaluation Test Stand
  - Develop ASIC test boards to build the test stand for production test
  - MicroBooNE FE ASIC production test took ~2 months
  - SBND will have 2.7x ASICs
  - Each test board has 4 ASIC sockets to speed up the chip test
  - Clam-shell style of socket to ease the chip handling

Cold Electronics



- FE ASIC Test Board
  - DAC: TI 16-bit DAC8411 is used to inject test pulse
  - ADC: Linear Tech 14-bit 4.5Msps LTC2314 is used to digitize analog output signal
  - Readout, DAQ, control and monitoring is through DUNE 35T FPGA mezzanine
    - No hardware development is necessary
  - Layout design is finished and ready for fabrication

Cold Electronics



- ADC ASIC Test Board
  - DAC: TI 16-bit quad channel DAC3484
  - Readout, DAQ, control and monitoring is through an FPGA evaluation board
    - DUNE 35T FPGA mezzanine doesn't have enough I/O pins
  - Schematics design will start once the interface to the FPGA evaluation board is finalized

FE/ADC Chip Production Plan in FY17

- SBND and protoDUNE will need 2,000 FE ASICs and ~2,000 ADC ASICs
  - 704 for SBND + 960 for protoDUNE + 20% spares
- Two options (no overhead is included)
  - Option 1: MPW run with additional wafers
    - ~$150k for FE ASIC and ~$150k for ADC ASIC, total ~$300k
    - ~$50k for MPW run, 50 additional wafers (40 chips per wafer) @ ~$2k each
  - Option 2: Dedicated run with additional wafers
    - ~$250k for both FE and ADC ASICs
    - One mask for both FE and ADC ASICs
    - ~$200k for mask of dedicated run, 25 additional wafers (180 FE + 180 ADC chips per wafer) @ $2k each
    - Will get ~5,000 chips for each ASIC

FE/ADC Chip Production Plan for DUNE 10kt

- DUNE 10kt will need ~30,000 FE ASICs and ~30,000 ADC ASICs
  - 24,000 for DUNE + 20% spares
- Option is to have a dedicated run with additional wafers (no overhead is included)
  - ~$550k for both FE and ADC ASICs
  - One mask for both FE and ADC ASICs
  - Assuming new mask for fine tuning of FE and ADC design based on protoDUNE results
  - ~$200k for mask of dedicated run, 175 additional wafers (180 FE + 180 ADC chips per wafer) @ $2k each
  - Will get ~32,000 chips for each ASIC

Contribution from Collaboration

- Collaboration efforts are important to bring up the integration test stand, perform QA test on production ASICs and boards
  - MicroBooNE has much stronger collaboration support compared to 35ton
- SBND and protoDUNE will need strong collaboration support as well for QA test of ASICs and boards
  - Collaborators are welcome to BNL/CERN/FNAL to perform production test
- DUNE 10kt will need better shared responsibility of QA test on production ASICs and boards
  - Multiple (3 ~ 5) production sites should be established for cold electronics production test
- Integration test stand should be maintained at major institutes (BNL/CERN/FNAL) for QA from protoDUNE though the last DUNE 10kt

Summary

- Key developments for LAr TPC projects share many commonalities in basic technical aspects
- We plan to build a full cold readout system, from TPC electrode to the signal feed-through, for system test of APA
  - QA procedure of individual components will be established along this development
  - Resources should be shared and optimized between SBND and DUNE
- System integration, in both SBND and protoDUNE at CERN, will serve as crucial steps toward a successful construction of DUNE
  - All experiments should benefit from both scientific and technical developments from each one of them